ISP1501

Universal Serial Bus 2.0 peripheral transceiver

Rev. 01 — 14 July 2000 **Objective specification**

1. General description

The ISP1501 is a full-function transceiver designed to provide a USB 2.0 analog front-end to Application-Specific Integrated Circuits (ASICs) and Field Programmable Gate Arrays (FPGAs) with a built-in USB Serial Interface Engine (SIE). A USB 2.0 transceiver is integrated to implement USB connectivity for high-speed peripherals. In addition, a USB 1.1 transceiver provides backward compatibility with full-speed USB systems. A minimum number of external components is needed.

2. Features

- Complies with *Universal Serial Bus Specification Rev. 2.0*
- Legacy compliant USB 1.1 full-speed transceiver interface
- Bus-powered capability with suspend mode
- Integrated parallel-to-serial converter (transmit) and serial-to-parallel converter (receive) for USB 2.0 data
- USB data recovery upon receiving
- USB data synchronization upon transmitting
- Integrated bit stuffing and de-stuffing
- Non-Return-to-Zero Inverted (NRZI) encoding and decoding
- Integrated Phase Locked Loop (PLL) oscillator using 12 MHz crystal
- Internal power-on reset
- Separate 3.3 V supplies for analog transceiver and digital I/Os minimizes crosstalk
- 16-bit bidirectional data bus allows FPGA verification, greatly reducing ASIC implementation risk
- Full industrial operating temperature range from –40 to +85 °C
- 8 kV in-circuit ESD protection for lower cost of external components
- Available in LQFP48 package.

3. Applications

- Scanner
- Digital still camera
- Printer, e.g.
  - Colour printer
  - Multi-functional printer
- External storage device, e.g.
  - Portable hard disk
  - Zip® drive
  - Jaz® drive
  - Magneto-optical (MO) drive
  - Optical drive (CD-ROM, CD-RW, DVD).

4. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
ISP1501BE	LQFP48	plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm	SOT313-2

5. Block diagram

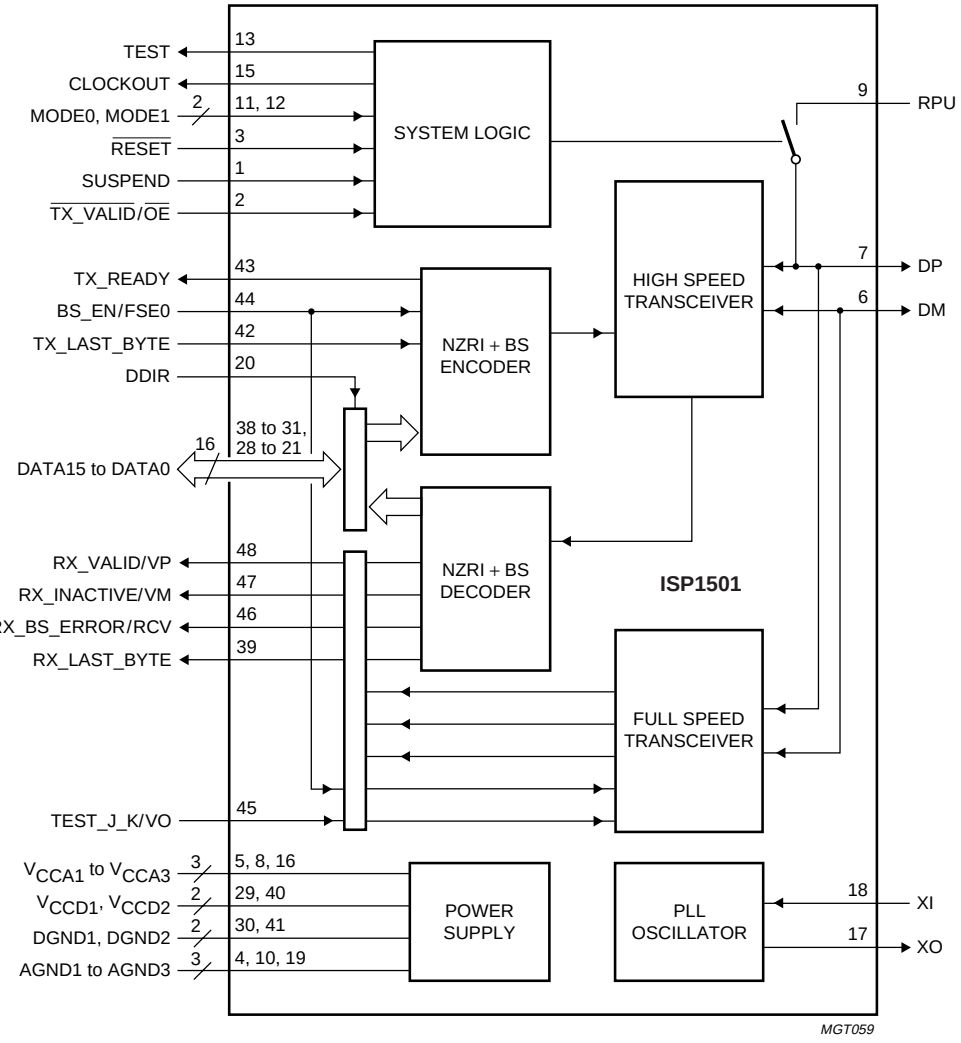


Fig 1. Block diagram.

6. Pinning information

6.1 Pinning

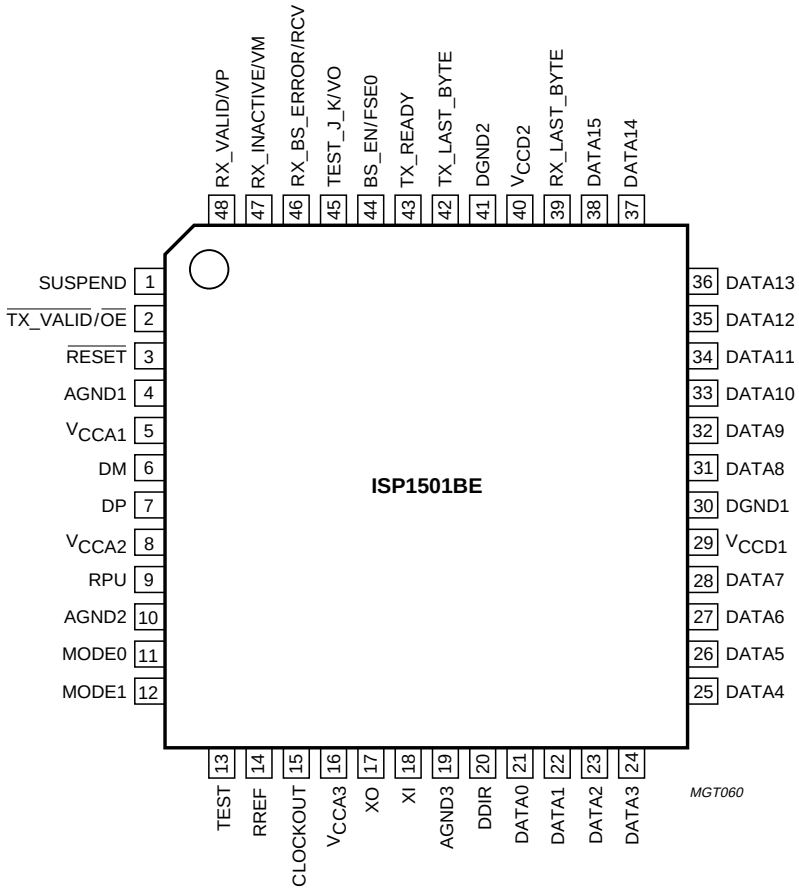


Fig 2. Pin configuration LQFP48.

6.2 Pin description

Table 2: Pin description

Symbol [1]	Pin	Type	Description
SUSPEND	1	I	enables power saving mode for USB bus suspend state
$\overline{TX\_VALID}$/$\overline{OE}$	2	I	pin function depends on operating mode (see Table 3): **State = 0, 1 —** output enable for FS transceiver [2] **State = 2, 3 —** transmission valid flag for HS transceiver [2]
$\overline{RESET}$	3	I	reset input
AGND1	4	-	analog ground supply
V_{CCA1}	5	-	analog supply voltage (3.3 V)
DM	6	AI/O	USB D– connection (analog) with integrated 45 Ω series resistor

Table 2: Pin description...*continued*

Symbol [1]	Pin	Type	Description
DP	7	AI/O	USB D+ connection (analog) with integrated 45 Ω series resistor
V_{CCA2}	8	-	analog supply voltage (3.3 V)
RPU	9	AI	connection for external pull-up resistor on USB D+; switched on via internal switch during FS state
AGND2	10	-	analog ground supply
MODE0	11	I	operating state and interface selection input; see Table 3
MODE1	12	I	operating state and interface selection input; see Table 3
TEST	13	O	test output; leave unconnected in normal operation
RREF	14	AI	connection for external reference resistor (12.2 kΩ ± 0.1%) to analog ground supply
CLOCKOUT	15	O	output clock for de-serialized data (30 MHz); clock is always running when input SUSPEND is logic 0
V_{CCA3}	16	-	analog supply voltage (3.3 V)
XO	17	AO	crystal oscillator output (12 MHz)
XI	18	AI	crystal oscillator input (12 MHz)
AGND3	19	-	analog ground supply
DDIR	20	I	selects data bus direction (logic 0 = output, logic 1 = input)
DATA0	21	I/O	data bit 0; bi-directional, slew rate controlled output (5 ns)
DATA1	22	I/O	data bit 1; bi-directional, slew rate controlled output (5 ns)
DATA2	23	I/O	data bit 2; bi-directional, slew rate controlled output (5 ns)
DATA3	24	I/O	data bit 3; bi-directional, slew rate controlled output (5 ns)
DATA4	25	I/O	data bit 4; bi-directional, slew rate controlled output (5 ns)
DATA5	26	I/O	data bit 5; bi-directional, slew rate controlled output (5 ns)
DATA6	27	I/O	data bit 6; bi-directional, slew rate controlled output (5 ns)
DATA7	28	I/O	data bit 7; bi-directional, slew rate controlled output (5 ns)
V_{CCD1}	29	-	digital supply voltage (3.3 V)
DGND1	30	-	digital ground supply
DATA8	31	I/O	data bit 8; bi-directional, slew rate controlled output (5 ns)
DATA9	32	I/O	data bit 9; bi-directional, slew rate controlled output (5 ns)
DATA10	33	I/O	data bit 10; bi-directional, slew rate controlled output (5 ns)
DATA11	34	I/O	data bit 11; bi-directional, slew rate controlled output (5 ns)
DATA12	35	I/O	data bit 12; bi-directional, slew rate controlled output (5 ns)
DATA13	36	I/O	data bit 13; bi-directional, slew rate controlled output (5 ns)
DATA14	37	I/O	data bit 14; bi-directional, slew rate controlled output (5 ns)
DATA15	38	I/O	data bit 15; bi-directional, slew rate controlled output (5 ns)
RX_LAST_BYTE	39	O	**logic 0 —** DATA[7:0] = bit stuff error byte, DATA[15:8] = valid data. **logic 1 —** DATA[7:0] = valid data, DATA[15:8] = bit stuff error byte
V_{CCD2}	40	-	digital supply voltage (3.3 V)
DGND2	41	-	digital ground supply

Table 2: Pin description *...continued*

Symbol [1]	Pin	Type	Description
TX_LAST_BYTE	42	I	transmit last byte input; a logic 1 causes DATA[7:0] to be sent as data (last byte) and DATA[15:8] to contain End Of Packet (EOP); input TX_BS_EN must be logic 1
TX_READY	43	O	transmit ready output; a logic 1 signals that valid data are available at the next rising edge on pin CLOCKOUT
BS_EN/ FES0	44	I	pin function depends on operating state (see Table 3): **State = 0, 1 —** a logic 1 forces single-ended zero (SE0) for FS transmitter **State = 2, 3 —** a logic 1 enables bit stuffing for the HS receiver and transmitter
TEST_J_K/ VO	45	I	pin function depends on operating state (see Table 3): **State = 0, 1 —** a logic 1 selects differential data at D+/D– receiver output **State = 2, 3 —** a logic 1 enables USB 2.0 test modes TEST_J and TEST_K; it also disables bit stuffing and NRZI for the HS receiver and transmitter
RX_BS_ERROR/ RCV	46	O	pin function depends on operating state (see Table 3): **State = 0, 1 —** differential data at D+/D– receiver output **State = 2, 3 —** a logic 1 signals a bit stuff error on receive data; the position of the erroneous byte is indicated by RX_LAST_BYTE
RX_INACTIVE/ VM	47	O	pin function depends on operating state (see Table 3): **State = 0, 1 —** single-ended D– receiver output **State = 2, 3 —** a logic 1 indicates HS line inactivity
RX_VALID/ VP	48	O	pin function depends on operating state (see Table 3): **State = 0, 1 —** single-ended D+ receiver output **State = 2, 3 —** valid data on rising clock edge at pin CLOCKOUT

[1] Symbol names with an overscore (e.g. $\overline{\text{NAME}}$) indicate active LOW signals.

[2] FS: full-speed (USB 1.1); HS: high-speed (USB 2.0).

7. Functional description

The incoming differential signal from the USB cable is amplified before it is fed to a sampler circuit. After oversampling the serial data is Non-Return-to-Zero-Inverted (NRZI) decoded and bit de-stuffed before being converted to 16-bit parallel words. These are then transferred to the decoder logic.

A squelch circuit detects high-speed activity on the line and activates the high-speed logic only when necessary.

Outgoing 16-bit parallel data words are first serialized, bit-stuffed and NRZI encoded. Then they are output to the USB cable via a differential driver circuit.

An internal bandgap reference circuit is used for generating the driver current and the biasing of the analog circuits. This circuit requires an external precision resistor (12.2 kΩ ± 0.1%) to analog ground.

An adaptive termination circuit ensures a correct 45 Ω termination for DP and DM. Calibration is done at power-on and when switching from FS to HS mode.

A PLL oscillator using a 12 MHz crystal generates the internal sampling clock of 480 MHz. From this signal a 30 MHz clock is derived for external use (available at pin CLOCKOUT).

An internal Power On Reset (POR) circuit monitors the digital supply and is used to start all circuits in the correct mode. An external reset can be applied via pin $\overline{\text{RESET}}$.

8. Operating states

8.1 Interface and state selection

The MODE1 and MODE0 pins control the operating states of ISP1501 and select the appropriate function of multiplexed pins (see Table 3).

Table 3: Interface selection

MODE[1:0]	State #	State name	Pin	Function
00	0	Disconnect	2	$\overline{\text{OE}}$
			44	FSE0
			45	VO
			46	RCV
			47	VM
			48	VP
01	1	Full-speed (FS)	2	$\overline{\text{OE}}$
			44	FSE0
			45	VO
			46	RCV
			47	VM
			48	VP

Table 3: Interface selection *...continued*

MODE[1:0]	State #	State name	Pin	Function
10	2	High-speed (HS)	2	$\overline{\text{TX\_VALID}}$
			44	BS_EN
			45	TEST_J_K
			46	RX_BS_ERROR
			47	RX_INACTIVE
			48	RX_VALID
11	3	High-speed chirp	2	$\overline{\text{TX\_VALID}}$
			44	BS_EN
			45	TEST_J_K
			46	RX_BS_ERROR
			47	RX_INACTIVE
			48	RX_VALID

8.2 State transitions

A USB 2.0 peripheral handles more than one electrical state under the USB specification. The ISP1501 accommodates the various states through the MODE[1:0] input pins. Table 4 summarizes the operating states and Figure 3 shows the state transition diagram.

When V_{BUS} is removed, the USB 2.0 peripheral must release the pull-up resistor on the DP pin (under Section 7.1.5 of the *USB Specification Rev. 2.0*). This is called the Disconnect state.

When a USB cable is connected from the USB 2.0 peripheral to the host controller, the peripheral defaults to the Full-speed (FS) state until it sees a bus reset from the host controller.

During bus reset, the peripheral initiates a high-speed chirp to detect whether the host controller supports USB 2.0 or USB 1.1. Chirping must be done with the DP pull-up resistor connected and the termination resistors on (DP/DM) disabled. This state is the High-speed chirp state. If the high-speed handshake shows a high-speed host is connected, the peripheral switches to the High-speed (HS) state.

In HS state the USB 2.0 peripheral must observe the bus for periodic activity. If the bus remains inactive for 3 ms, the peripheral switches to the FS state to check for an SE0 (single-ended zero) condition on the USB bus.

If an SE0 is detected within the designated time window (100 to 875 µs, see section 7.1.7.6 of the *USB Specification Rev. 2.0*), the peripheral switches to the HS Chirp state to do a high-speed detection handshake. Otherwise, the peripheral remains in the FS state with adherence to bus-suspend rules.

The peripheral remains in the FS state until a HS resume brings it to the HS state without going through reset (see section 7.1.7.7 of the *USB Specification Rev. 2.0*). The peripheral may also initiate a Remote wake-up to resume the bus.

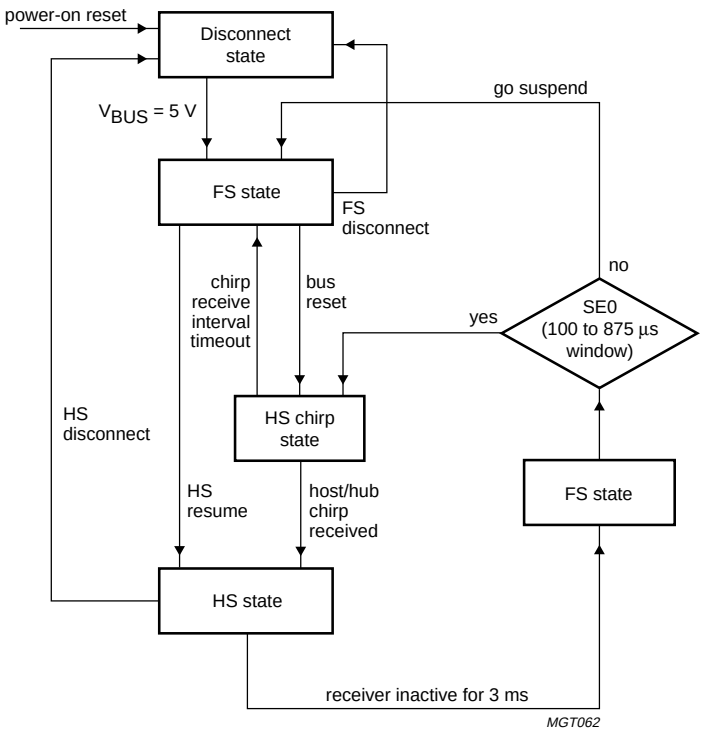


Fig 3. State transition diagram.

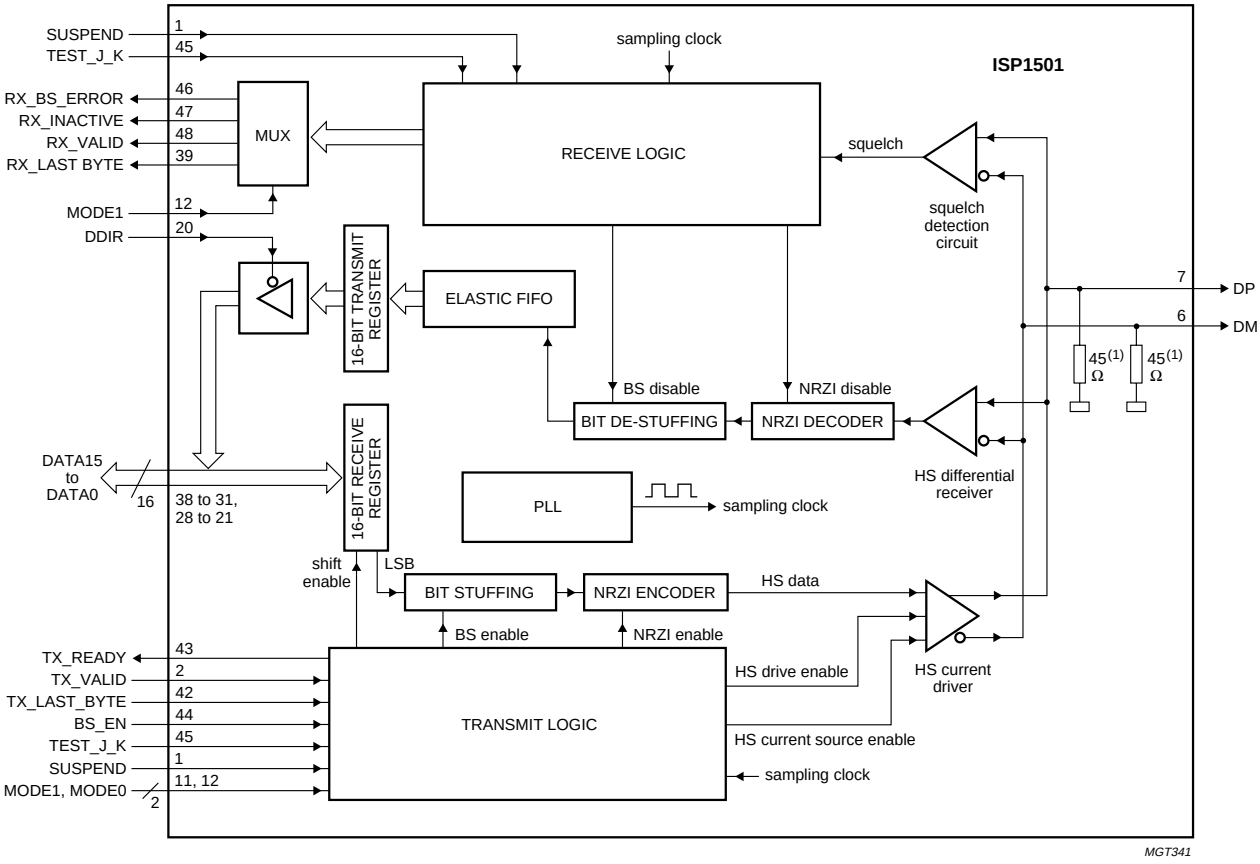
Table 4: Operating states

State #	State name	Description
0	Disconnect	Legacy (full-speed) SIE interface; FS transceiver enabled; pull-up resistor on pin RPU disconnected
1	Full-speed (FS)	Legacy (full-speed) SIE interface; FS transceiver enabled; full-speed slew rate selected; pull-up resistor on pin RPU connected to pin DP
2	High-speed (HS)	High-speed SIE interface; HS transceiver enabled; FS transceiver on permanent SE0; pull-up resistor on pin RPU disconnected
3	High-speed chirp	High-speed SIE interface; high-speed transceiver enabled; full-speed transceiver disabled; pull-up resistor on pin RPU connected to pin DP

8.3 Disconnect state

In Disconnect state (MODE[1:0] = 00) the external pull-up resistor on pin RPU is not connected to the DP line. This prevents current from leaking into a connected host that is powered off. The FS transceiver is enabled and the legacy (USB 1.1) SIE interface is active.

9. High-speed functionality



(1) Implemented as part of FS transceiver.

Fig 4. High-speed transceiver functional diagram.

9.1 High-speed transmit

The ISP1501 must be set in high-speed state by setting MODE[1:0] to 02H. High-speed data propagate to the DP and DM pins when the 16-bit input data bus is driven. Driving pin DDIR to logic 1 switches the 16-bit data bus to input mode.

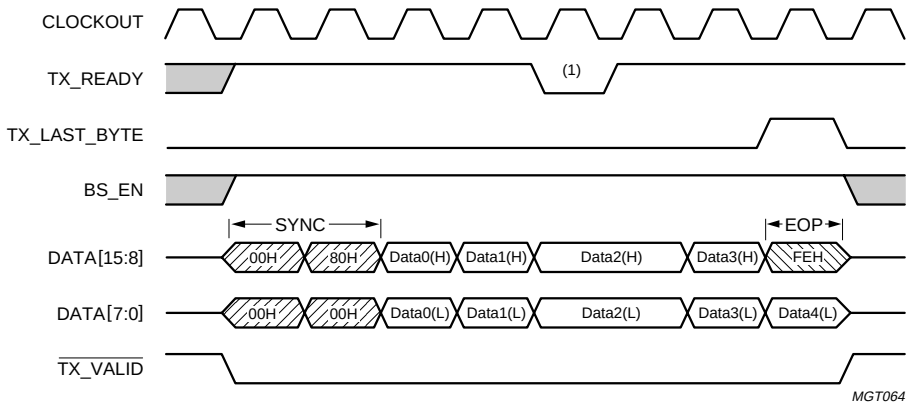
All data packets start with a 4-byte SYNC pattern and end with either a 1-byte or a 5-byte EOP (End of Packet). The SYNC pattern is a 32-bit pattern of KJKJKJKJ KJKJKJKJ KJKJKJKJ KJKJKJKK, which is sent as 0000H, 8000H to the input. For a 1-byte EOP the HS pattern is generated with FEH. The 5-byte EOP starts with FEH, followed by four bytes of FFH.

Remark: All 16-bit data are sent LSB first.

When bit stuffing or the EOP finishes on an 8-bit boundary, the BS_EN and TX_LAST_BYTE determine the behavior of the ISP1501 as shown in Table 5.

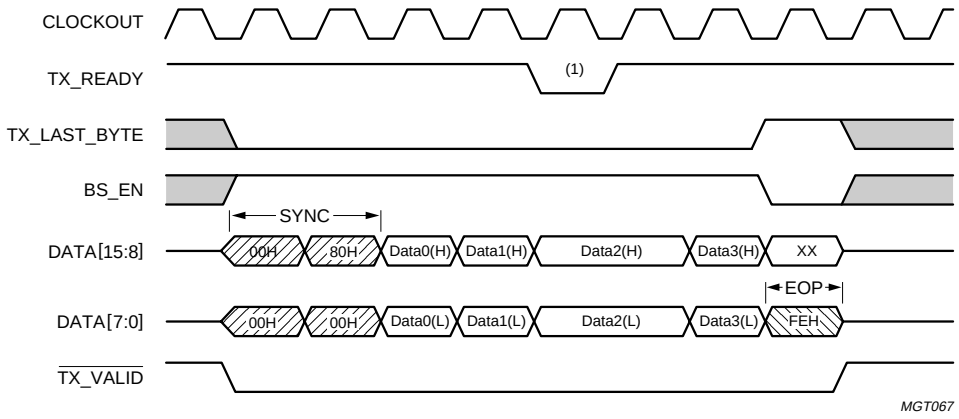
Table 5: High-speed transmit conditions

TX_LAST_BYTE	BS_EN	Condition
0	0	high and low byte are both sent without bit stuffing
0	1	high and low byte are both sent with bit stuffing
1	0	low byte is sent without bit stuffing; high byte is ignored
1	1	low byte is sent with bit stuffing, high byte without bit stuffing



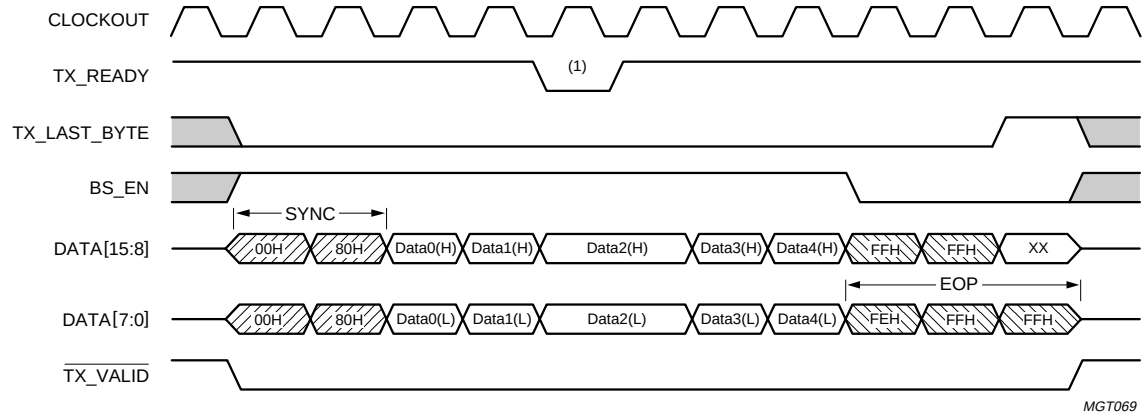
(1) TX_READY is only de-asserted during a transmission if the internal FIFO is full.

Fig 5. HS transmit; single-byte EOP ending on 16-bit boundary.



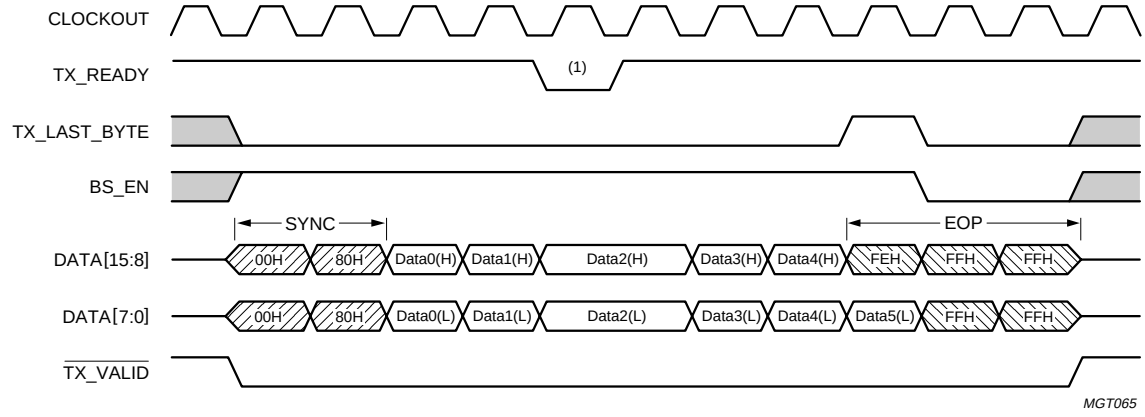
(1) TX_READY is only de-asserted during a transmission if the internal FIFO is full.

Fig 6. HS transmit; single-byte EOP ending on 8-bit boundary.



(1) TX_READY is only de-asserted during a transmission if the internal FIFO is full.

Fig 7. HS transmit; 5-byte EOP ending on 8-bit boundary.



(1) TX_READY is only de-asserted during a transmission if the internal FIFO is full.

Fig 8. HS transmit; 5-byte EOP ending on 16-bit boundary

9.2 High-speed receive

When ISP1501 is in high-speed state (MODE[1:0] = 02H), setting input DDIR to logic 0 allows the HS receiver to output data to the external 16-bit bus. As the length of the incoming EOP is not fixed, RX_LAST_BYTE and RX_BS_ERROR are encoded to differentiate between EOP arriving on an 8-bit or a 16-bit boundary. RX_VALID qualifies the **data** part of USB high-speed traffic.

If the EOP arrives on the high byte, RX_VALID will qualify it, and RX_LAST_BYTE will be asserted. With these, the SIE will know that an EOP has occurred and can start deciphering the received packet.

If the EOP arrives on a 16-bit word boundary, RX_VALID goes LOW at the start of the EOP cycle. RX_BS_ERROR must be polled to determine whether an EOP has occurred.

Table 6: High-speed receive conditions

RX_LAST_BYTE	RX_BS_ERROR	Condition
0	0	valid data on high and low byte; no bit stuff error
0 [1]	1 [1]	2 bytes of EOP on high and low byte
1	0	EOP on high byte, valid data on low byte
1	1	illegal, will never occur

[1] This condition is only valid in the cycle immediately after pin RX_VALID goes LOW.

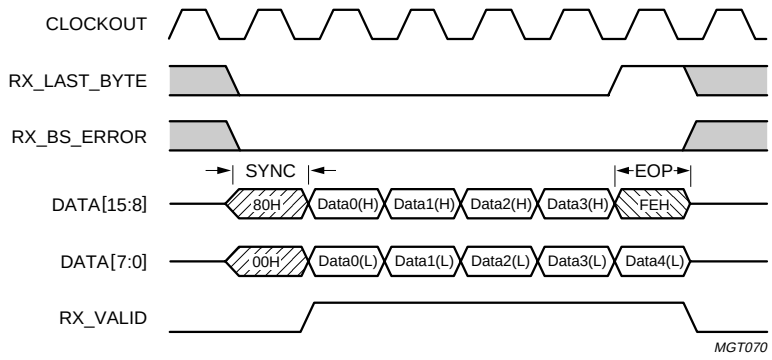


Fig 9. HS receive timing; single-byte EOP ending on 16-bit boundary.

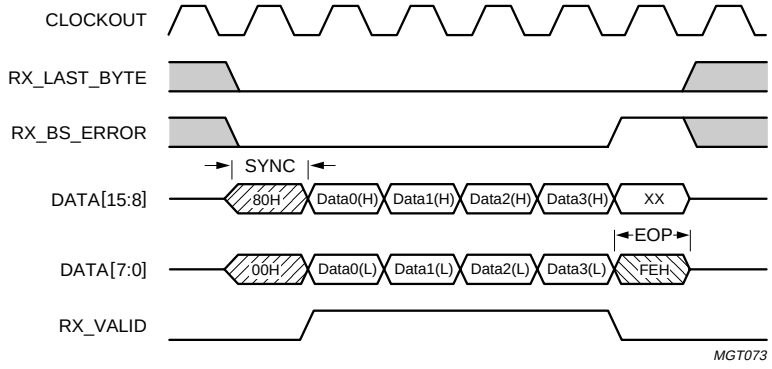


Fig 10. HS receive timing; single-byte EOP ending on 8-bit boundary.

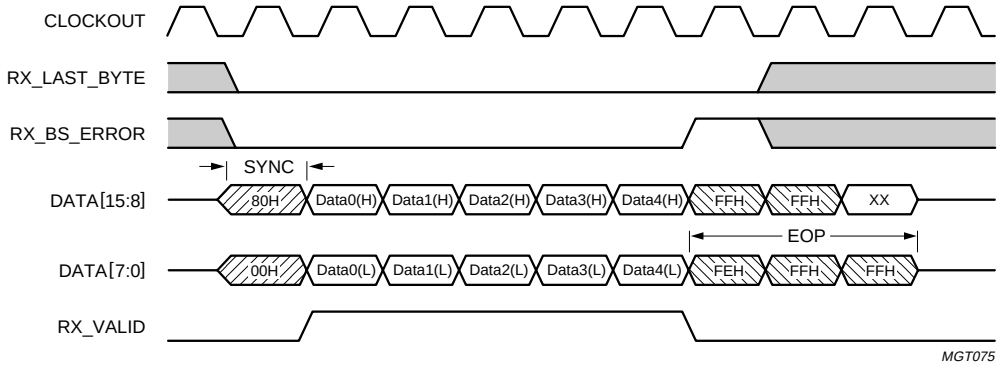


Fig 11. HS receive timing; 5-byte EOP ending on 8-bit boundary.

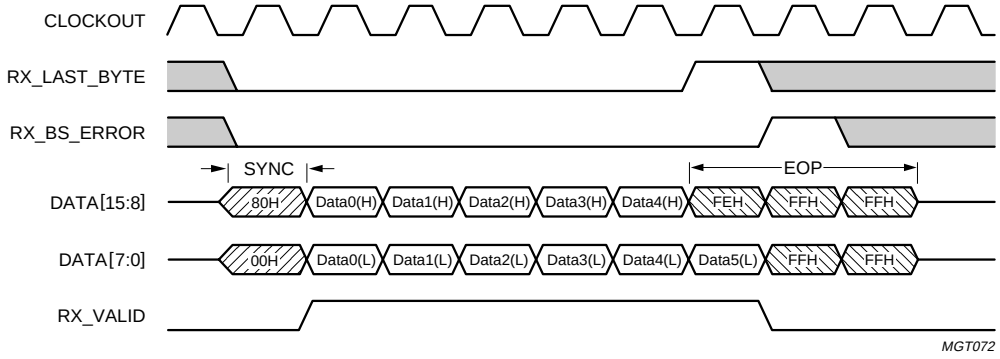


Fig 12. HS receive timing; single-byte EOP ending on 16-bit boundary.

The SYNC pattern will not appear on the data bus as an RX_VALID qualified data. The received SYNC value may differ from the expected 8000H due to bit errors.

The raw data is byte-aligned to the 16-bit data bus. The received EOP is also propagated to the 16-bit data bus.

9.3 High-speed chirp

When the transceiver is configured to high-speed chirp state (MODE[1:0] = 03H), the internal termination resistors on DP and DM are deactivated (no SE0 is applied by the FS transceiver). The DP pin is connected to the pull-up resistor on pin RPU. No bit stuffing or NRZI encoding is performed on the data, regardless of the state of pin BS_EN. The data is transmitted as soon as both TX_VALID_N and TX_READY are asserted, see Figure 13.

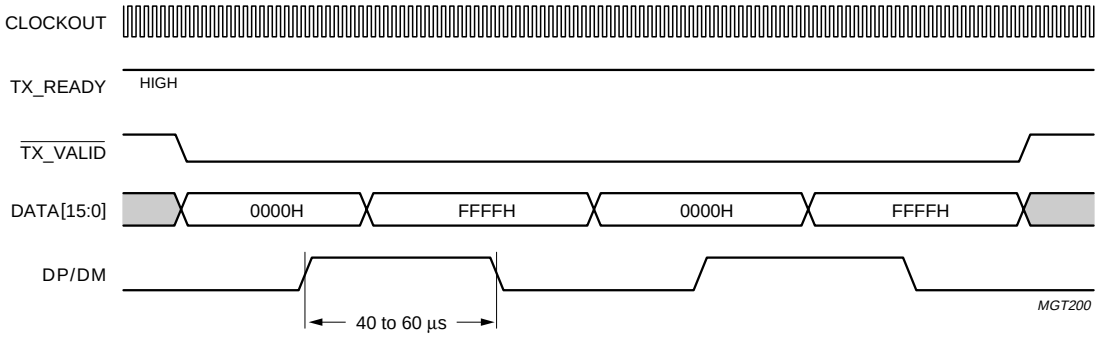


Fig 13. HS chirp transmit timing.

For high-speed chirp reception, the 16-bit data bus is in bypass mode. RX_VALID no longer qualifies the input data. The SIE samples the 16-bit parallel data to check for the presence of extended JKJK states. RX_BS_EN no longer reflects a bit stuff error.

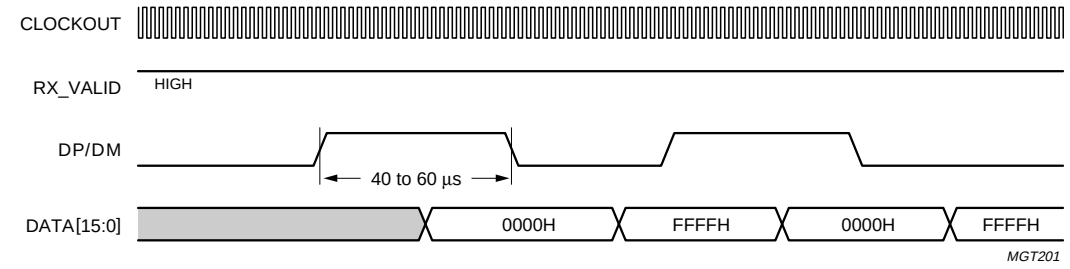


Fig 14. HS chirp receive timing.

9.4 High-speed transmit path delay

The total transmit path maximum delay is 37 bits at 480 MHz.

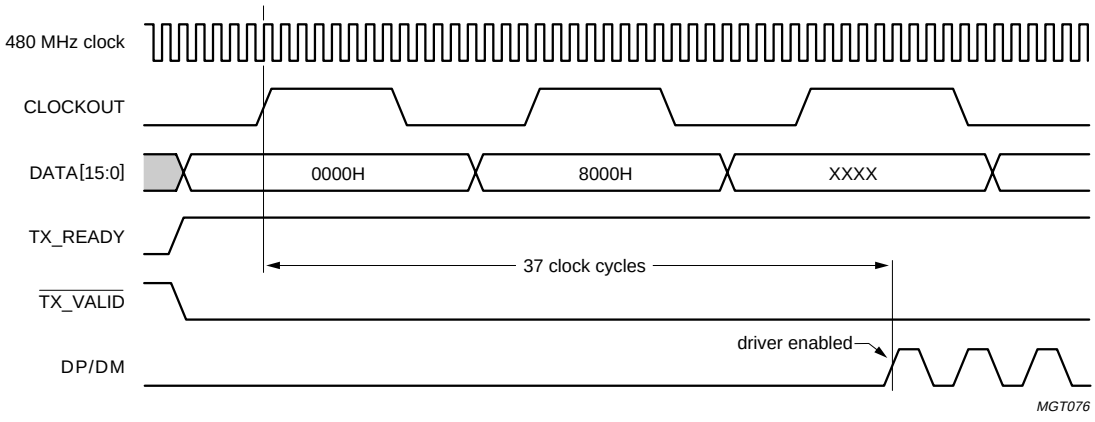


Fig 15. HS transmit path delay.

9.5 High-speed receive path delay

In HS receive mode the SYNC packet is removed. As the preceding SYNC packet may be trimmed, the delay from the appearance of the first bit of valid data to the first valid data word on the DATA[15:0] bus is described here.

However, to have an accurate measure of the bus turn-around time, the receive path delay is measured from the data on the (DP, DM) pins to the actual equivalent data on the 16-bit data bus.

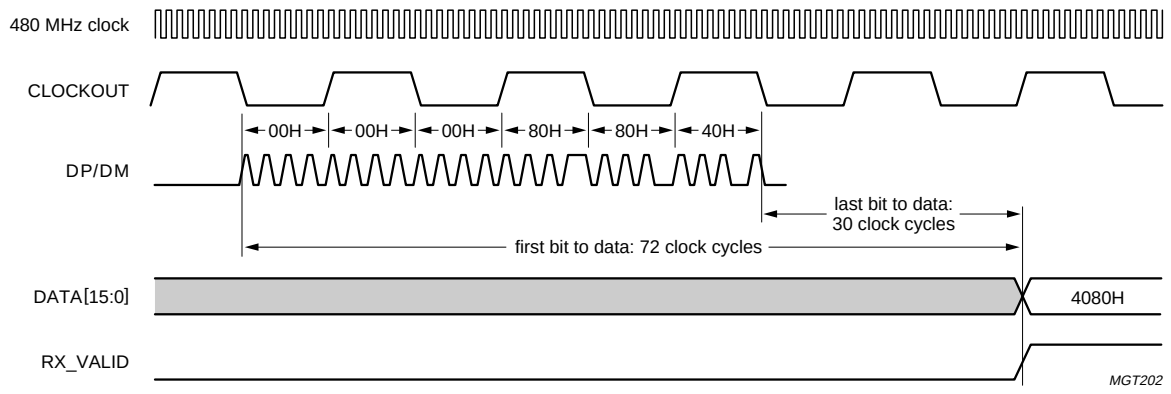


Fig 16. HS receive path delay.

10. Full-speed functionality

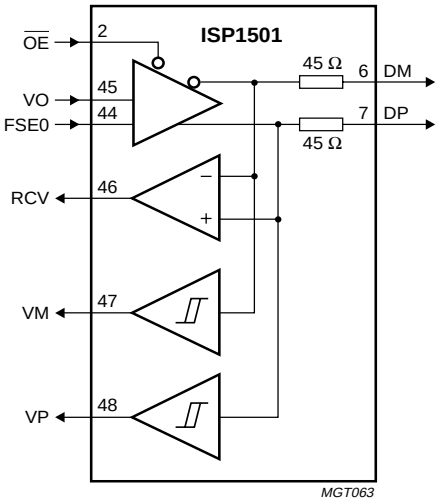


Fig 17. Full-speed transceiver functional diagram

Table 7: Full-speed driving function

$\overline{OE}$ = logic 0

FSE0	VO	VP	VM	Differential data (DP, DM)
0	0	0	1	full-speed K state
0	1	1	0	full-speed J state
1	0	0	0	SE0
1	1	0	0	SE0

Table 8: Full-speed receiving function

$\overline{OE}$ = logic 1

Differential input	Single-ended input		VP	VM	RCV [1]
$\Delta V = V_{DP} - V_{DM}$	V_{DP}	V_{DM}			
ΔV > 200 mV	> 2 V	< 0.8 V	1	0	1
ΔV < –200 mV	< 0.8 V	> 2 V	0	1	0
$\lvert\Delta V\rvert$ < 200 mV	< 0.8 V	< 0.8 V	0	0	RCV* [2]

[1] When a logic 1 is applied at input SUSPEND, output RCV is always made logic 0.

[2] RCV* denotes the signal level on output RCV just before the SE0 state occurs. This level is kept stable during the SE0 period.

11. Limiting values

Table 9: Absolute maximum ratings

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCA}	analog supply voltage		–0.5	+6.0	V
V_{CCD}	digital supply voltage		–0.5	+4.6	V
V_I	input voltage		–0.5	+6.0	V
$I_{latchup}$	latchup current	$-1.8 < V_I < 5.4$	-	100	mA
V_{esd}	electrostatic discharge voltage [1]	$I_{LI} < 1$ µA	-	±2000 [2]	V
T_{stg}	storage temperature		–40	+125	°C

[1] Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ resistor (Human Body Model).

[2] For pins D+ and D– the values for V_{esd} are ±8000 V (air discharge) and ±4000 V (contact discharge), using a capacitor of 150 pF and a 330 Ω resistor.

Table 10: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCA}	analog supply voltage		3.0	3.3	3.6	V
V_{CCD}	digital supply voltage		3.0	3.3	3.6	V
V_I	input voltage		0	-	V_{CCD}	V
$V_{I(AI/O)}$	input voltage on analog I/O pins (DP, DM)		0	-	3.6	V
T_{amb}	operating ambient temperature		–40	-	+85	°C

12. Static characteristics

Table 11: Static characteristics: supply pins

$V_{CCA} = V_{CCD} = 3.0$ to 3.6 V; $V_{AGND} = V_{DGND} = 0$ V; $T_{amb} = -40$ to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	operating supply current	full-speed transmitting and receiving at 12 MHz; 50 pF load on (DP, DM)	-	<tbd>	6	mA
		high-speed receiving at 480 MHz	-	<tbd>	54	mA
		high-speed transmitting at 480 MHz	-	<tbd>	100	mA
$I_{CC(susp)}$	suspend supply current	in suspend mode with 1.5 kΩ pull-up resistor on pin RPU disconnected	-	-	40	µA

Table 12: Static characteristics: digital pins

V_{CCA} = V_{CCD} = 3.0 to 3.6 V; V_{AGND} = V_{DGND} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input levels						
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
Output levels						
V_{OL}	LOW-level output voltage	I_{OL} = 100 µA	-	-	0.15	V
		I_{OL} = 4 mA	-	-	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = 100 µA	V_{CCD} − 0.4	-	-	V
		I_{OH} = 4 mA	V_{CCD} − 0.4	-	-	V
Leakage current						
I_{LI}	input leakage current		-	-	±1	µA

Table 13: Static characteristics: analog I/O pins (DP/DM)

V_{CCA} = V_{CCD} = 3.0 to 3.6 V; V_{AGND} = V_{DGND} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
USB 1.1 transceiver (FS)						
Input levels (differential receiver)						
V_{DI}	differential input sensitivity	$\|V_{I(DP)} - V_{I(DM)}\|$	0.2	-	-	V
V_{CM}	differential common mode voltage	includes V_{DI} range	0.8	-	2.5	V
Input levels (single-ended receivers)						
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{hys}	hysteresis voltage		0.4	-	0.7	V
Output levels						
V_{OL}	LOW-level output voltage	pull-up on DP; R_L = 1.5 kΩ to + 3.6 V	-	-	0.3	V
V_{OH}	HIGH-level output voltage	pull-down on DP, DM; R_L = 15 kΩ to GND	2.8	-	3.6	V
USB 2.0 transceiver (HS)						
Input levels (differential receiver)						
V_{HSSQ}	high-speed squelch detection threshold (differential)	squelch detected	-	-	100	mV
		no squelch detected	150	-	-	mV
V_{HSDSC}	high-speed disconnect detection threshold (differential)	disconnect detected	625	-	-	mV
		disconnect not detected	-	-	525	mV
V_{HSDI}	high-speed differential input sensitivity	$\|V_{I(DP)} - V_{I(DM)}\|$	300	-	-	mV
V_{HSCM}	high-speed data signaling common mode voltage range		−50	-	+500	mV
Output levels						
V_{HSOI}	high-speed idle level output voltage (differential)		−10	-	+10	mV
V_{HSOL}	high-speed LOW-level output voltage (differential)		−10	-	+10	mV

Table 13: Static characteristics: analog I/O pins (DP/DM) *...continued*

V_{CCA} = V_{CCD} = 3.0 to 3.6 V; V_{AGND} = V_{DGND} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{HSOH}	high-speed HIGH-level output voltage (differential)		360	-	440	mV
V_{CHIRPJ}	chirp-J output voltage (differential)		[1] 700	-	1100	mV
V_{CHIRPK}	chirp-K output voltage (differential)		[1] −900	-	−500	mV
Leakage current						
I_{LZ}	OFF-state leakage current		-	-	±1	µA
Capacitance						
C_{IN}	transceiver capacitance	pin to GND	-	-	20	pF
Resistance						
Z_{DRV2} [2]	driver output impedance for USB 2.0 and USB 1.1	steady-state drive	40.5	45	49.5	Ω
Z_{INP}	input impedance		10	-	-	MΩ
Termination						
V_{TERM}	termination voltage for pull-up resistor on pin RPU		3.0 [3]	-	3.6	V

[1] HS termination resistor disabled, pull-up resistor connected. Only during reset, when both hub and device are high-speed capable.

[2] Includes internal matching resistors on both DP and DM. This tolerance range complies to USB 2.0.

[3] In 'suspend' mode the minimum voltage is 2.7 V.

13. Dynamic characteristics

Table 14: Dynamic characteristics: analog I/O pins (DP/DM)

V_{CCA} = V_{CCD} = 3.0 to 3.6 V; V_{AGND} = V_{DGND} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver characteristics						
High-speed mode						
t_{HSR}	high-speed differential rise time		500	-	-	ps
t_{HSF}	high-speed differential fall time		500	-	-	ps
Full-speed mode						
t_{FR}	rise time	C_L = 50 pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$; see Figure 18	4	-	20	ns
t_{FF}	fall time	C_L = 50 pF; 90 to 10% of $\|V_{OH} - V_{OL}\|$; see Figure 18	4	-	20	ns
FRFM	differential rise/fall time matching (t_{FR}/t_{FF})	excluding the first transition from Idle state	90	-	111.1	%
V_{CRS}	output signal crossover voltage	excluding the first transition from Idle state; see Figure 19	1.3	-	2.0	V

Table 14: Dynamic characteristics: analog I/O pins (DP/DM) *…continued*

V_{CCA} = V_{CCD} = 3.0 to 3.6 V; V_{AGND} = V_{DGND} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Low-speed mode						
t_{LR}	rise time	C_L = 200 to 600 pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$; see Figure 18	75	-	300	ns
t_{LF}	fall time	C_L = 200 to 600 pF; 90 to 10% of $\|V_{OH} - V_{OL}\|$; see Figure 18	75	-	300	ns
LRFM	differential rise/fall time matching (t_{LR}/t_{LF})	excluding the first transition from Idle state	80	-	125	%
V_{CRS}	output signal crossover voltage	excluding the first transition from Idle state; see Figure 19	1.3	-	2.0	V
Driver timing						
High-speed mode (Template 1, *Universal Serial Bus Specification Rev. 2.0*)						
-	driver waveform requirements	eye pattern of Template 1; see Figure 23 [1]		see Table 15		
Full-speed mode						
$t_{PLH(drv)}$	driver propagation delay (VO, FSE0 to DP, DM)	LOW-to-HIGH; see Figure 21	-	-	15	ns
$t_{PHL(drv)}$		HIGH-to-LOW; see Figure 21	-	-	15	ns
t_{PHZ}	driver disable delay ($\overline{OE}$ to DP, DM)	HIGH-to-OFF; see Figure 19	-	-	10	ns
t_{PLZ}		LOW-to-OFF; see Figure 19	-	-	10	ns
t_{PZH}	driver enable delay ($\overline{OE}$ to DP, DM)	OFF-to-HIGH; see Figure 19	-	-	15	ns
t_{PZL}		OFF-to-LOW; see Figure 19	-	-	15	ns
Low-speed mode						
Not specified: low-speed delay timings are dominated by the slow rise/fall times t_{LR} and t_{LF}.						
Receiver timing						
High-speed mode (Template 4, *Universal Serial Bus Specification Rev. 2.0*)						
-	data source jitter and receiver jitter tolerance	eye pattern of Template 4; see Figure 24 [1]		see Table 16		
Full-speed and low-speed mode						
Differential receiver						
$t_{PLH(rcv)}$	receiver propagation delay (DP, DM to RCV)	LOW-to-HIGH; see Figure 20	-	-	15	ns
$t_{PHL(rcv)}$		HIGH-to-LOW; see Figure 20	-	-	15	ns
Single-ended receiver						
$t_{PLH(se)}$	single-ended propagation delay (DP, DM to VP, VM)	LOW-to-HIGH; see Figure 20	-	-	15	ns
$t_{PHL(se)}$		HIGH-to-LOW; see Figure 20	-	-	15	ns

[1] Characterized only, not tested in production. Limits guaranteed by design.

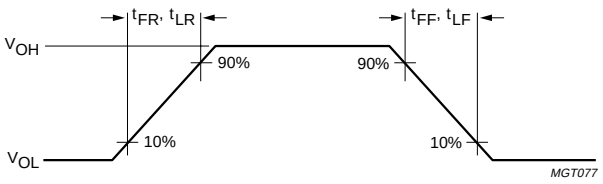


Fig 18. Rise and fall times (FS and LS mode).

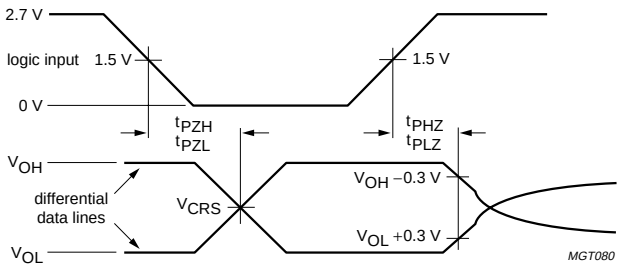


Fig 19. Timing of $\overline{OE}$ to DP, DM.

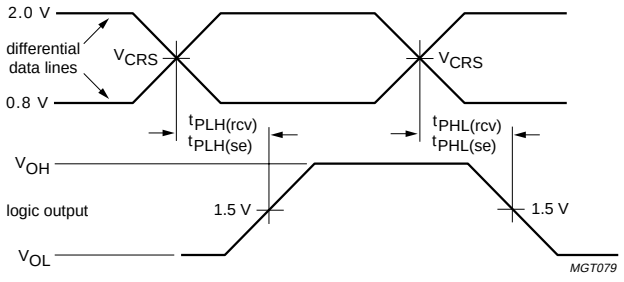


Fig 20. Timing of DP, DM to RCV, VP, VM.

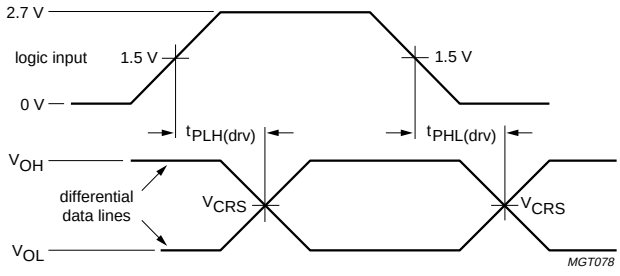


Fig 21. Timing of VO, FSE0 to DP, DM.

13.1 High-speed signals

High-speed USB signals are characterized using eye patterns. For measuring the eye patterns 4 test points have been defined (see Figure 22). The *Universal Serial Bus Specification Rev. 2.0* defines the eye patterns in several ‘templates’. For ISP1501 only Templates 1 and 4 are relevant.

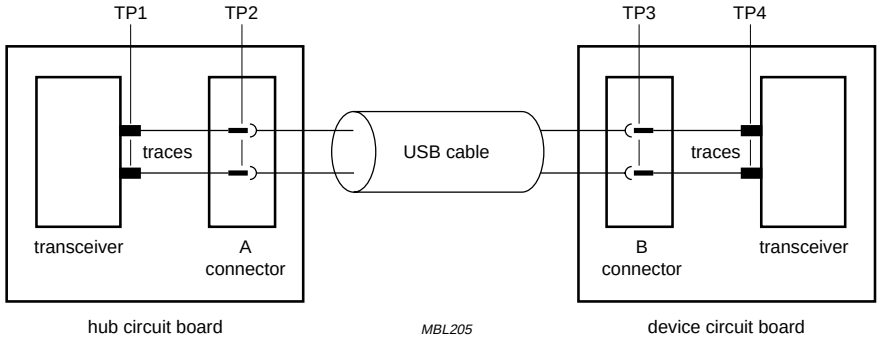


Fig 22. Eye pattern measurement planes.

13.1.1 Template 1 (transmit waveform)

The eye pattern in Figure 23 defines the transmit waveform requirements for a hub (measured at TP2) or a device without a captive[1] cable (measured at TP3). The corresponding signal levels and timings are given in Table 15. Timings are given as a percentage of the unit interval (UI), which represents the nominal bit duration T_{PERIOD} for a 480 Mbit/s transmission rate.

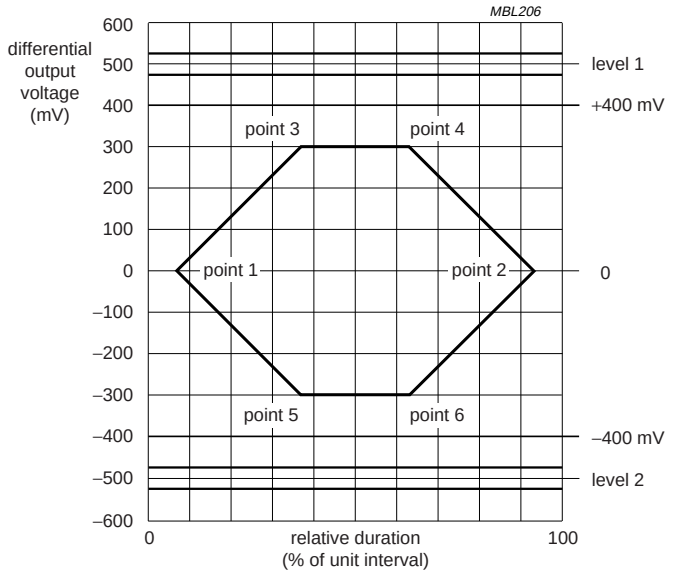


Fig 23. Template 1 eye pattern (transmit waveform).

Table 15: Template 1 eye pattern definition

Name	Differential voltage on DP, DM (mV)	Relative duration (% of unit interval)
Level 1	+525 [1] +475 [2]	n.a.
Level 2	–525 [1] –475 [2]	n.a.
Point 1	0	7.5
Point 2	0	92.5
Point 3	+300	37.5
Point 4	+300	62.5
Point 5	–300	37.5
Point 6	–300	62.5

[1] In the unit interval following a transition.

[2] In all other cases.

1. Captive cables have a vendor-specific connector to the peripheral (hardwired or detachable) and a USB “A” connector on the other side. For hot plugging, the vendor-specific connector must meet the same performance requirements as a USB “B” connector.

13.1.2 Template 4 (receive waveform)

The eye pattern defined in Table 16 defines the receiver sensitivity requirements for a hub (signal applied at test point TP2) or a device without a captive cable (signal applied at test point TP3). The corresponding signal levels and timings are given in Table 16. Timings are given as a percentage of the unit interval (UI), which represents the nominal bit duration T_{PERIOD} for a 480 Mbit/s transmission rate.

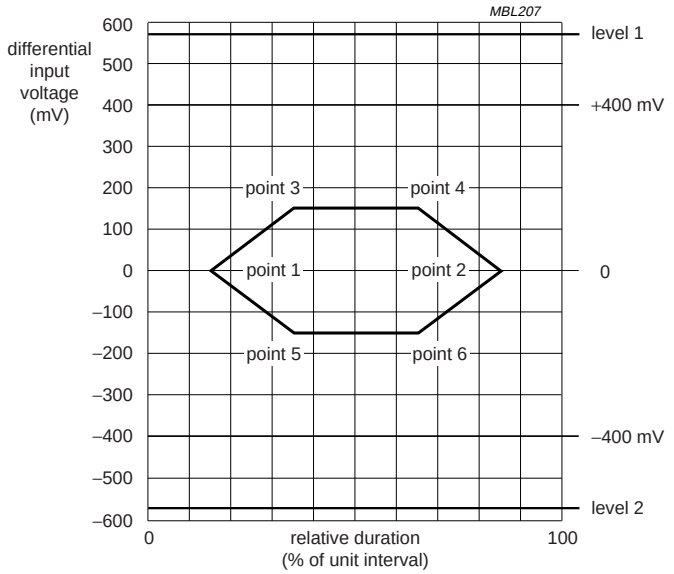


Fig 24. Template 4 eye pattern (receive waveform).

Table 16: Template 4 eye pattern definition

Name	Differential voltage on DP, DM (mV)	Relative duration (% of unit interval)
Level 1	+575	n.a.
Level 2	−575	n.a.
Point 1	0	15
Point 2	0	85
Point 3	+150	35
Point 4	+150	65
Point 5	−150	35
Point 6	−150	65

14. Parallel digital interface timing

14.1 High-speed transmit timing

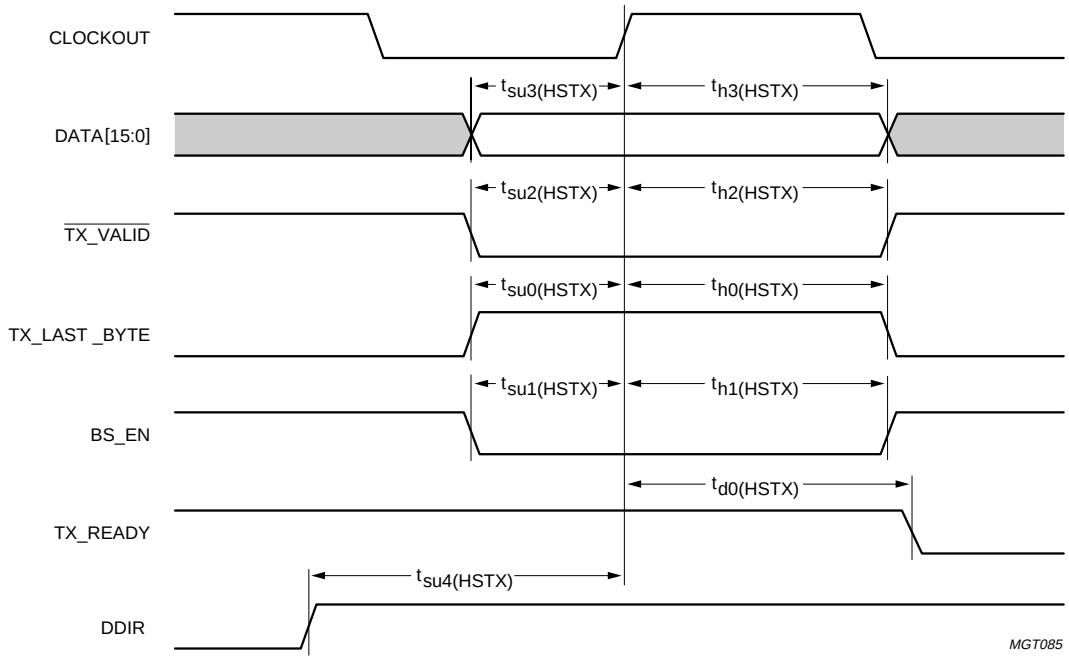


Fig 25. Parallel digital interface timing: high-speed transmit.

Table 17: High-speed transmit timing

CLOCKOUT duty cycle = 50%; see Figure 25

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{su3(HSTX)}$	data setup time to rising clock edge		6.6	-	-	ns
$t_{h3(HSTX)}$	data hold time after rising clock edge		0.1	-	-	ns
$t_{su0(HSTX)}$	$\overline{TX\_VALID}$ setup time to rising clock edge		6.6	-	-	ns
$t_{su1(HSTX)}$	BS_EN setup time to rising clock edge		6.6	-	-	ns
t_{su2}(HSTX)	TX_LAST_BYTE setup time to rising clock edge		6.6	-	-	ns
$t_{h0(HSTX)}$	$\overline{TX\_VALID}$ hold time after rising clock edge		0.1	-	-	ns
$t_{h1(HSTX)}$	BS_EN hold time after rising clock edge		0.1	-	-	ns

Table 17: High-speed transmit timing...*continued*

CLOCKOUT duty cycle = 50%; see Figure 25

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{h2}(HSTX)	TX_LAST_BYTE hold time after rising clock edge		0.1	-	-	ns
t_{su4}(HSTX)	DDIR switching time before rising clock edge		8.1	-	-	ns
t_{d0}(HSTX)	TX_READY output delay after rising clock edge		-	-	6.9	ns

14.2 High-speed receive timing

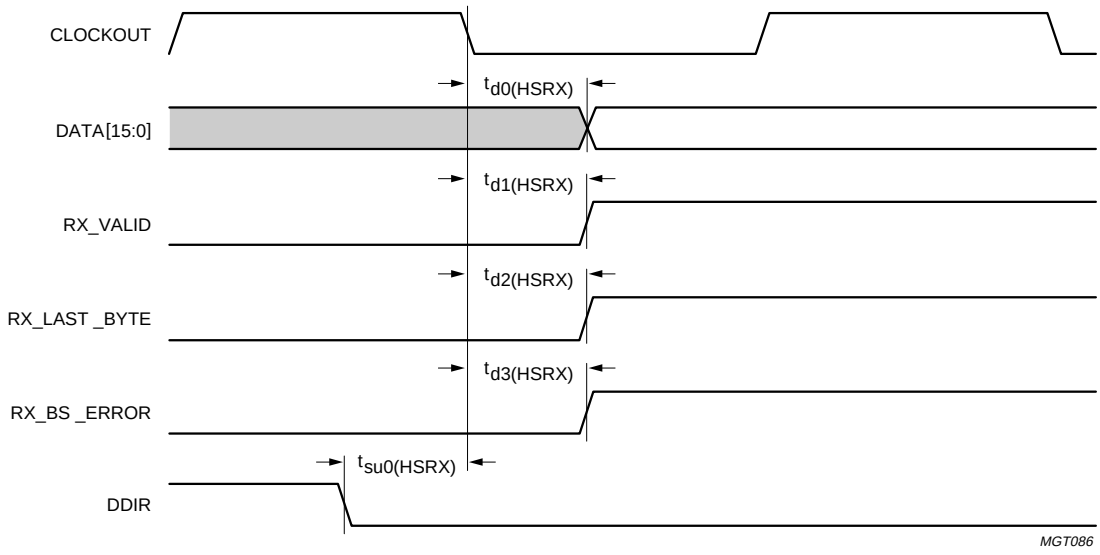


Fig 26. Parallel digital interface timing: high-speed receive.

Table 18: High-speed receive timing

CLOCKOUT duty cycle = 50%; see Figure 26

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{su4}(HSRX)	DDIR switching time before falling clock edge		3.3	-	-	ns
t_{d0}(HSRX)	received data output delay after falling clock edge		-	-	6.8	ns
t_{d1}(HSRX)	RX_VALID delay after falling clock edge		-	-	6.8	ns
t_{d2}(HSRX)	RX_LAST_BYTE delay after falling clock edge		-	-	6.8	ns
t_{d3}(HSRX)	RX_BS_ERROR delay after falling clock edge		-	-	6.8	ns

15. Application information

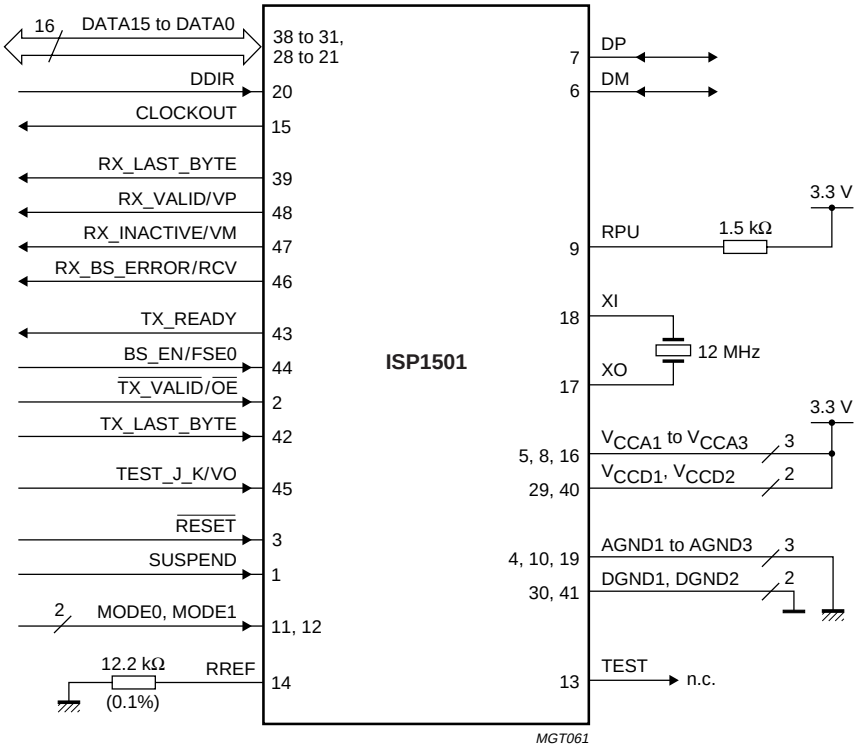
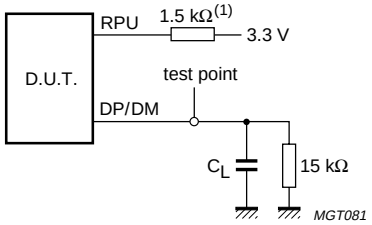


Fig 27. Application diagram.

16. Test information



(1) Internally connected to pin DP, depending on the selected operating state (see Table 4).

Fig 28. FS test fixture.

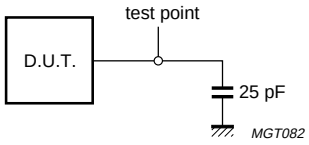
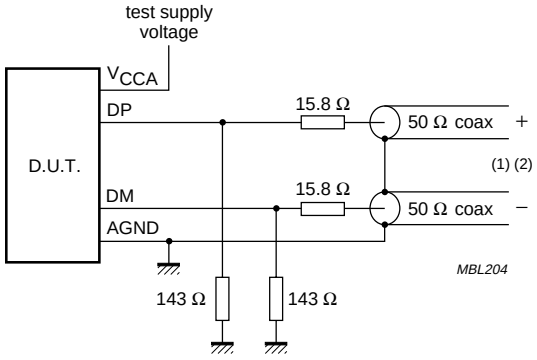


Fig 29. Load for VM, VP and RCV in FS mode.



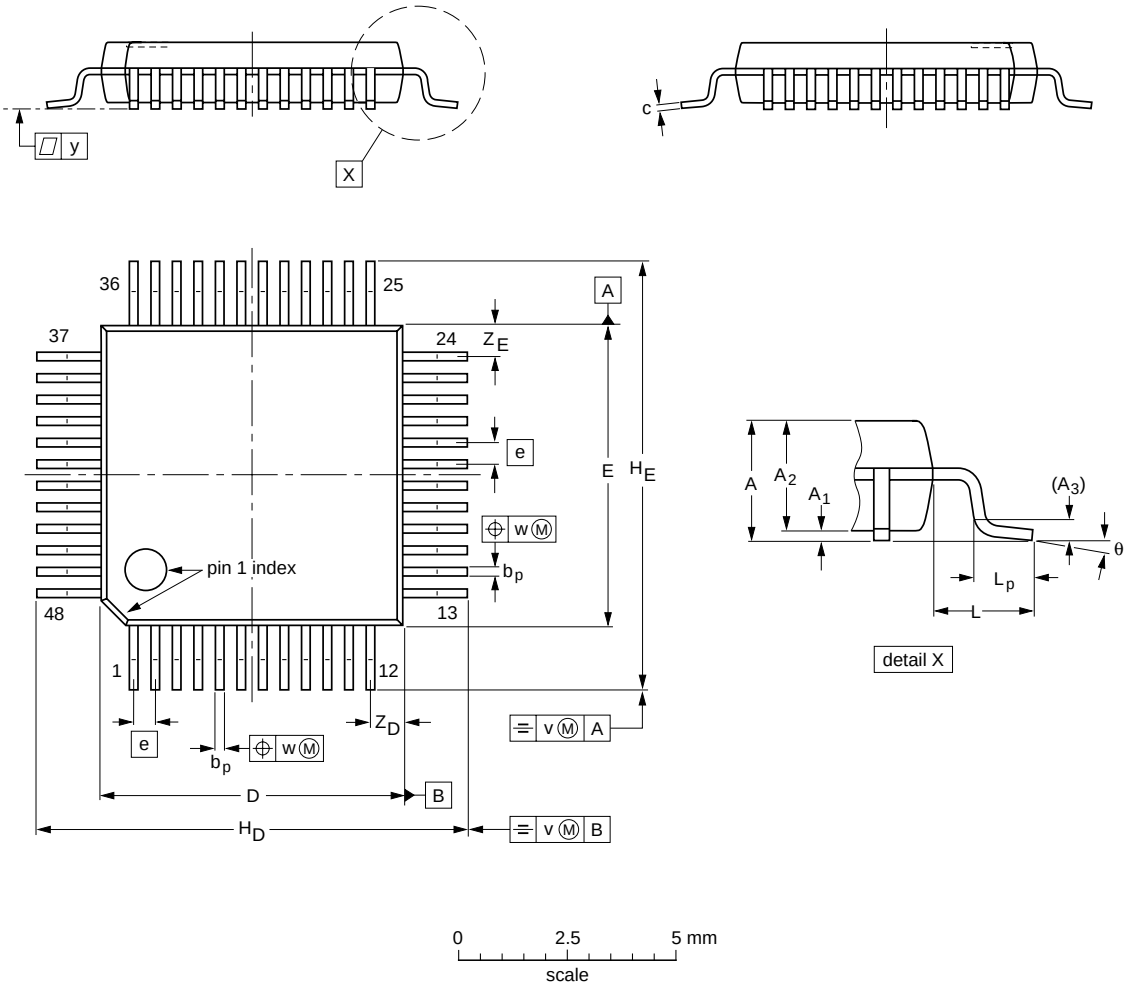
(1) Transmitter: connected to 50 Ω inputs of a high-speed differential oscilloscope.

(2) Receiver: connected to 50 Ω outputs of a high-speed differential data generator.

Fig 30. High-speed transmitter/receiver test fixture.

17. Package outline

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2	136E05	MS-026				~~99-12-27~~ 00-01-19

Fig 31. LQFP48 package outline.

18. Soldering

18.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

18.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

18.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

18.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

18.5 Package related soldering information

Table 19: Suitability of surface mount IC packages for wave and reflow soldering methods

Package	Soldering method	
	Wave	Reflow [1]
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable [2]	suitable
PLCC [3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [3] [4]	suitable
SSOP, TSSOP, VSO	not recommended [5]	suitable

[1] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[2] These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).

[3] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[4] Wave soldering is only suitable for LQFP, QFP and TQFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[5] Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

19. Revision history

Table 20: Revision history

Rev	Date	CPCN	Description
01	20000714		Objective specification; initial version.

20. Data sheet status

Datasheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

21. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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